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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/662,302	09/16/2003	Ennis T. Ogawa	TI-33455.1	1776
23494	7590	08/24/2005	EXAMINER	
TEXAS INSTRUMENTS INCORPORATED P O BOX 655474, M/S 3999 DALLAS, TX 75265			STEVENSON, ANDRE C	
			ART UNIT	PAPER NUMBER
			2812	
DATE MAILED: 08/24/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/662,302

Applicant(s)

OGAWA ET AL.

Examiner

Andre' C. Stevenson

Art Unit

2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 29 June 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 15-35 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 15-35 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 March 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_.

## Detailed Action

### *Response to Arguments*

Applicant's arguments filed March 21, 2005 have been fully considered but they are not persuasive. See below;

**Applicant Argues** that the terms "active diffusion volume" are defined in the specification at page 17, lines 5 to 9, by the simultaneous intersection of the interconnect volume diffusion volume, and stress gradient region at a specific site within a device structure. Hence, active diffusion volume is the smallest overlapping portion of the three volumes surrounding a vulnerable SIV site.

**Examiner** has considered the applicants argument but have not found it persuasive. The applicant states in the disclosure (pg. #4, line 15-21), that the problem of voids (SIV) exist in devices utilizing back-end technologies. Thus, although Yang does not mention explicitly "Active Diffusion Volume", it is still present in his invention utilizing backend technology. The Examiner takes the position that the claim language, as it is written now, reads on the invention of Yang.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this

Art Unit: 2812

subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 15-~~20~~<sup>35 ACS</sup> are rejected under 35 U.S.C. 102(e) as being anticipated by Yang et al.

(U.S. Pat. No. 6,468,894, Patented 10/22/02, Filed 03/21/01).

Yang shows, in figures 1-12 and corresponding text, in a method where damascene interconnects both electrically active and inactive are formed, with respect to **claim #15, 21 and 29**, pertaining to a semiconductor device structure comprising: a first metallic interconnect (**fig. 7, item 14 & fig 12, item 56**); a second metallic interconnect (**fig. 7, item 28 & fig. 12, item 64**) (**column 3, lines 45-67; column 4, lines 1-5; column 5, lines 18-30**); a primary via structure (**any one of item 30 in fig 7, or any one of item 70 in fig 12**), disposed between and electrically intercoupling the first and second metallic interconnects (**column 5, lines 31-40**); and a buffer structure (**fig. 7, item 32, 34 and 36, or any one of item 30 remaining from the primary via structure, or fig 12, item 68, 72 and 74, or any one of item 70 remaining from the primary via structure**), disposed upon the first metallic interconnect in proximity to the primary via structure, and adapted to buffer the primary via structure from diffusive voiding occurring at a contact point between the primary via structure and the first metallic interconnect (**column 5, lines 31-40; column 4, lines 30-50**). Note that the Examiner considers it inherent, that for example, items 32, 34, 36 and any one of 30, apart from the primary via structure, would buffer the primary structure from diffusive voiding in that the vias 32, 34 and 36 are “capable” of remedying the conventional prior art problem of diffusive voiding by providing alternatives to the primary via structure regarding diffusion issues. *Pertaining to Claim #16*, Yang also shows that the second metallic interconnect and the primary via structure are copper-based dual damascene structures. (**Fig. 8-12 item 62, 64 and 66; column 1, lines 47-**

Art Unit: 2812

**52; column 6, lines 22-33).** *Pertaining to claim #17*, Yang shows, wherein the buffer structure comprises a second via structure, disposed between and electrically intercoupling the first and second interconnects. **(Fig. 12, item 72, 74 and any one of item 70 remaining from the primary via structure; Fig 7, any one of item 30 remaining from the primary via structure; column 6, lines 22-33).** *Pertaining to claim 18*, Yang shows, wherein the buffer structure comprises a second, electrically inactive, via structure **(item 36)**, disposed upon the first metallic interconnect **(item 14)** proximal to the primary via structure **(Fig. 7)**. *Pertaining to claim #19*, Yang shows, wherein the buffer structure comprises of an electrically inactive structure disposed upon the first metallic interconnect to immediately and completely surround the primary via structure. **(Fig. 7-12, item 32, 34, 36, 68, 72; column 6, lines 22-33; column 5, lines 49-54).** *Pertaining to claim #20*, Yang shows, wherein the buffer structure comprises: a second via structure, disposed between and electrically intercoupling the first and second metallic interconnects **(any one of item 30 remaining from the primary via structure)**; and a third electrically inactive **(item 36)**, via structure, disposed upon the first metallic interconnect **(item 14)** proximal to the primary via structure **(column 5, lines 32-42 and lines 49-54)**. *Pertaining to claim #22*, Yang shows, wherein the redundant structure comprises plural redundant structures **(fig. #12; column 6, lines 22-33)**. *Pertaining to claim #23*, Yang shows, wherein the redundant structure is operative relative to diffusive redundancy only **(fig. #12; column 6, lines 22-33)**. *Pertaining to claim #24* Yang shows, wherein the redundant structure is operative relative to electrical redundancy **(fig. #12; column 6, lines 22-33)**. *Pertaining to claim #25*, Yang shows, 21 wherein said device has a copper-based, dual-damascene structure having an active diffusion volume within the dual-damascene structure relative to a location within the dual-damascene

Art Unit: 2812

structure to which voids can migrate (**fig. #8; column 3, lines 52-67; column 4, lines 1-5; column 5, lines 55-67**). *Pertaining to claim #26*, Yang shows, wherein said device has a copper-based, dual-damascene structure having an active diffusion volume within the dual-damascene structure relative to a location within the dual-damascene structure to which voids can migrate (**fig. #12; column 5, lines 55-65; column 6, lines 22-33**). *Pertaining to claim #27*, Yang shows, wherein said device has a copper-based, dual-damascene structure having an active diffusion volume within the dual-damascene structure relative to a location within the dual-damascene structure to which voids can migrate (**fig. #8; column 3, lines 52-67; column 4, lines 1-5; column 5, lines 55-67**). *Pertaining to claim #28*, Yang shows, wherein said device has a copper-based, dual-damascene structure having an active diffusion volume within the dual-damascene structure relative to a location within the dual-damascene structure to which voids can migrate (**fig. #8; column 3, lines 52-67; column 4, lines 1-5; column 5, lines 55-67**). *Pertaining to claim #30*, Yang shows, wherein said structure is at least one via extending from said first layer and spaced from said second layer (**Fig. 12, item 72, 74 and any one of item 70 remaining from the primary via structure; Fig 7, any one of item 30 remaining from the primary via structure; column 6, lines 22-33**). *Pertaining to claim #31*, Yang shows, wherein said at least one via is a plurality of vias (**fig. #12; column 6, lines 22-33**). *Pertaining to claim #32*, Yang shows, wherein said plurality of vias are equidistant from said via and spaced apart (**fig. #4; column 4, lines 30-50**). *Pertaining to claim #33*, Yang shows, wherein said structure is at least one electrically insulating slot disposed in said first layer and within said active diffusion volume (**column 3, lines 52-67; column 4, lines 1-5**). *Pertaining to claim #34*, Yang shows, wherein said at least one slot is a plurality of spaced apart slots (**fig. #4; column 4, lines 30-50**).

Art Unit: 2812

***Pertaining to claim #35***, Yang shows, wherein said structure further includes at least one electrically insulating slot disposed in said first layer and within said active diffusion volume (**Abstract; column 3, lines 52-67; column 4, lines 1-5**).).

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

### **Conclusion**

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure; Dirahoui et al. (U.S. Pat. No. 6,492,259), Chuang (U.S. Pat. No. 6,828,223), Motsiff et al. (U.S. Pat. No. 6,573,538), Hasegawa et al. (U.S. Pat. No. 6,452,274).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre' Stevenson whose telephone number is (571) 272 1683. The examiner can normally be reached on Monday through Friday from 7:30 am to 4:30 pm.

Art Unit: 2812

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt, can be reached on (571) 272 1873. The fax phone number for the organization where this application or proceeding is assigned is (703) 308 7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 0956. Also, the proceeding numbers can be used to fax information through the Right Fax system;

**(703) 872-9306**

Andre' Stevenson

08/18/05

  
MICHAEL LEBENTRITT  
SUPERVISORY PATENT EXAMINER